

# **28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages**

by

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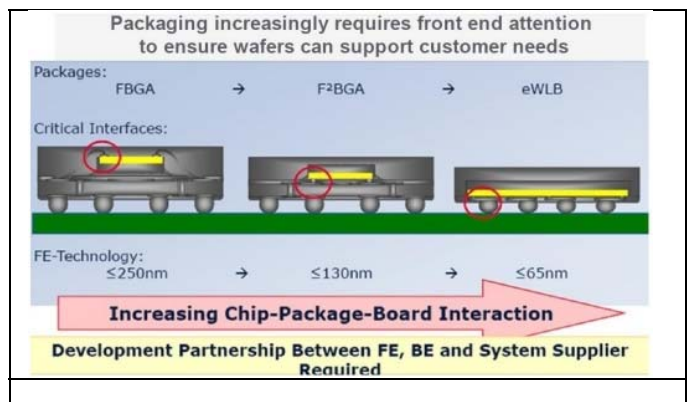
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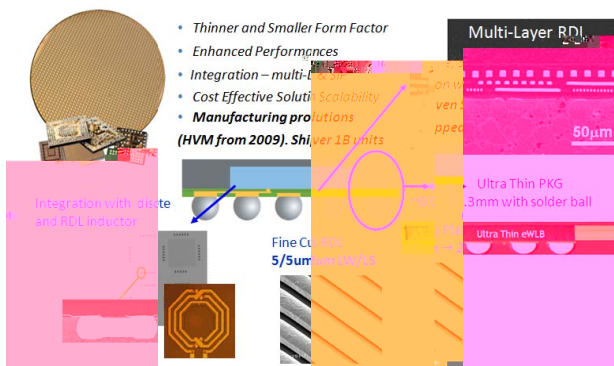
*Abstract*

I.



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***Advanced Wafer-Level Technology: eWLB/FOWLP***



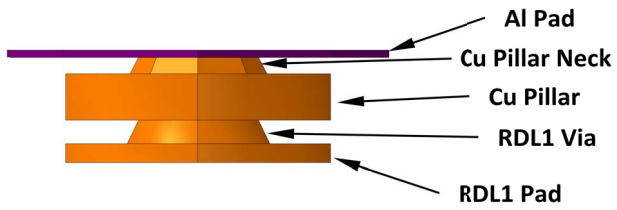
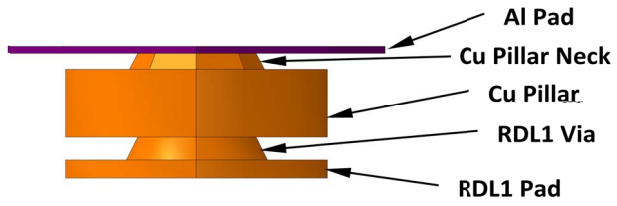
***II.***

***Test Vehicle Specification***

**Reliability Test**



**Via Shape**



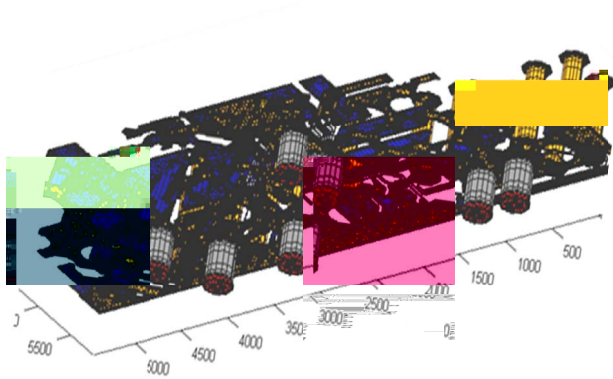
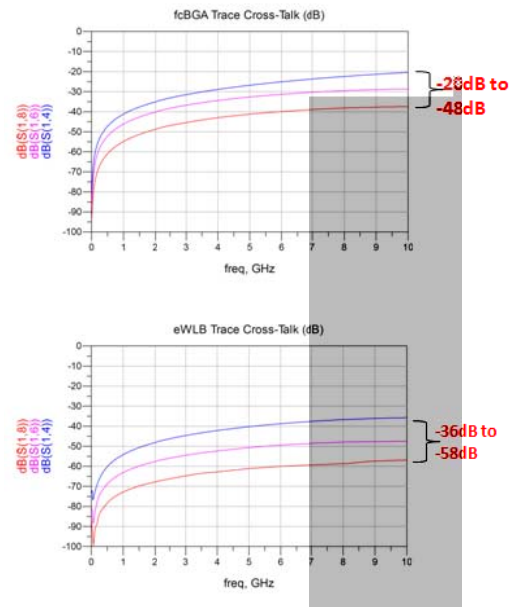
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Temperature (°C)	Design Option			
	1	2	3	4
250	1.00	0.91	0.87	0.79
125	1.00	0.93	1.15	1.20
25	1.00	0.88	1.04	1.09
-55	1.00	0.92	1.03	1.08

Electrical S

Thermal Characterization

1. High-speed bus with each trace impedance-matched (e.g., to 50 Ohm)
2. Trace lengths are typically between 2 -3 mm
3. Trace distance to GND plane: 50 um for laminate, and 5 um for eWLB
4. eWLB is very thin package. As a result, the cross-talk in eWLB is typically much lower, more than 10 dB



### III.

Net	Inductance, L (pH)			Resistance, R (mOhm)	
	flipchip	eWLB	$\Delta(\%)$	flipchip	eWLB
1	1.77	0.43	-75%	240	100
2	2.03	0.24	-88%	308	100
3	1.51	0.57	-62%	348	100
4	1.08	0.25	-77%	268	100

